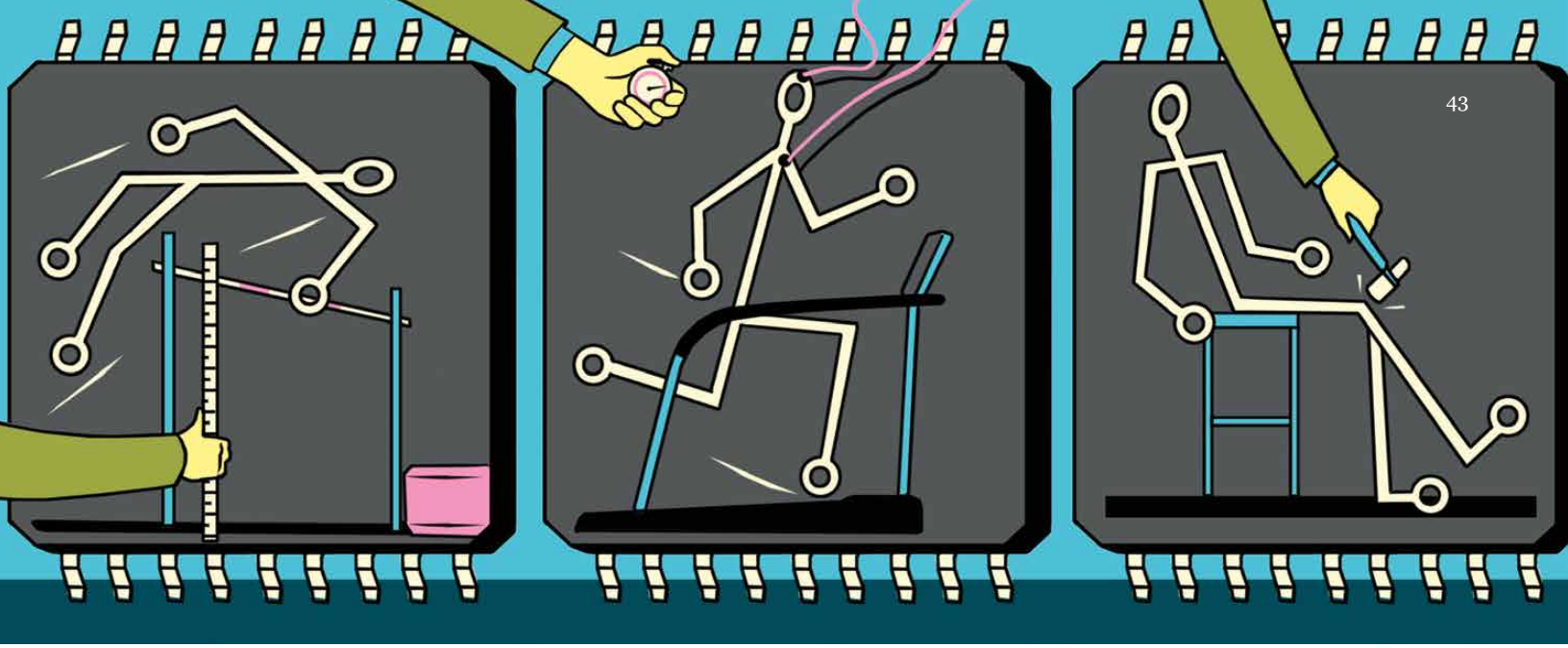

Bill Butcher

Standing up to the semiconductor verification challenge

Companies should seek faster, more cost-effective ways to test the quality of complex system-on-a-chip devices.

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The tail is wagging the dog in most system-on-a-chip (SOC) development efforts.

Design verification, the end-stage process of ensuring that everything on an integrated circuit works as planned, consumed more than 55 percent of the total time spent on a typical SOC design project in 2012, up from 49 percent in 2007, according to the Wilson Research Group's 2012 Functional Verification Study. This increase in time spent is a direct reflection of newer, more complex generations of semiconductors that have many more transistors and many more functions, all of which must be carefully vetted. Flaws that are found late in the production process, or not at all, can create poor customer experiences that can damage chip designers' reputations. So most companies have accepted the risk-versus-efficiency trade-off and are relying on conservative, resource-intensive approaches to design validation and testing. As a result, however, they are often forgoing potential profits from the timely release of their SOC devices. What's more, the demand for ever-increasing complexity in today's circuitry is not likely to slow down, so the percentage of total project time that must be spent on SOC verification will likely continue to increase—unless semiconductor companies rethink their approach.

An obvious first step is to assess and adopt testing technologies that can help streamline the

verification process. But some of these tools and techniques can be expensive to implement, particularly for smaller semiconductor players. So companies may also want to consider ways to simplify the verification tasks associated with a particular chip or family of chips and examine the steps they can take to improve the infrastructure they have set up to support verification efforts—for example, creating a centralized verification organization, with a dedicated senior leader, to oversee the testing process. Indeed, by enhancing their capabilities in three areas—technology, process, and organization—and by taking time to develop an overarching verification plan rather than tackling the verification process chip by chip, companies may significantly reduce both their time to market and the cost of development associated with their SOCs.

In this article, we consider the use of data analytics in verification-project planning and discuss ways to simplify integrated-circuit testing. We also look at the advantages of different verification technologies for different players, as well as ways to establish an organizational infrastructure that facilitates efficient SOC testing. These technology, process, and organizational levers can be used to complement—and jump-start—companies' traditional approaches to verification. Our study of productivity measures associated with more than 1,400 integrated-circuit projects suggests that, by streamlining the verification process, chip companies may be able to increase their productivity by at least 10 percent—for instance, by closing their design-specification stages faster, producing more SOC devices, and moving them to market more quickly. Such an approach could provide even small semiconductor players with a means to differentiate themselves from larger rivals.

The verification process

The traditional approach to verification begins after chip design is complete. The chip design is simulated via a "test bench," which consists of software code written in the hardware-description languages that a designer uses to test each functional block of an integrated circuit. The test bench instantiates the chip, supplies stimulus signals, and measures and evaluates the resulting responses from the chip. This process enables the test bench to determine whether the block meets predetermined specifications.

When dealing with a complex system on a chip, different designers typically will work on individual functional blocks within the chip, often following different schedules. Complications can arise because the designer working on functional block A often requires input from blocks B and C to verify his or her design. As SOCs have become more complex and the number of transistors on them continues to climb, managing these interrelationships has become increasingly unwieldy. And the task will not get any easier with the ongoing trend toward miniaturization.

Resolving the verification challenge

Our experience, industry research, and expert interviews suggest that semiconductor players often skimp on the time spent in verification planning. Put simply, design teams don't know what they don't know about their approach to verification and are therefore missing significant opportunities to improve aspects of this critical quality-control process. Teams will often focus most of their verification resources on executing the project and staying on schedule, leaving less time for up-front critical thinking (exhibit). As a result, they may not recognize the chances they have to save costs and create production

efficiencies by, for instance, reusing certain pieces of intellectual property or simplifying chip architectures. In the face of rising production costs and complexity, semiconductor players should take more, not less, time for planning, using readily available project and process data to set their verification objectives. Armed with this information, design teams can find ways to introduce simplicity into their verification processes and tailor their use of new technologies to specific verification situations rather than assuming one size fits all. The data can also inform companies' attempts to build a robust verification organization.

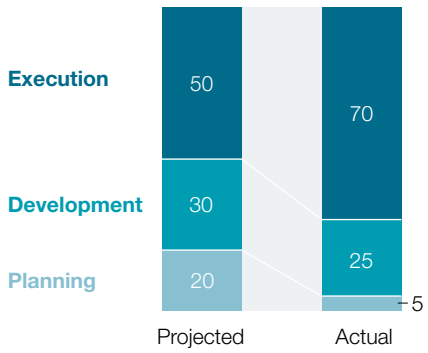
Use data analytics in planning discussions

Verification may happen late in chip development, but conversations about quality control should occur quite early and often. Companies should convene project-launch planning discussions, bringing together members of the verification team, leaders on individual projects, design engineers, and senior managers. The goal is to get an accurate read on the resources required to carry out verification tasks for every SOC in development, what the testing schedule should look like, and the potential risks associated with certain SOCs or families of chips. Input from members of the verification team in these conversations will be crucial; they will have the institutional knowledge required to make qualified estimates. Advanced analytics can play an important role here, as it now does in decision-making processes across most industries. Using historical project and process information, semiconductor players can develop a comprehensive verification-process database that, over time, will allow senior managers to see where and when critical pain points are likely to emerge in the typical verification process and react accordingly. The data and planning discussions can also help companies determine how much verification is enough—often, the decision about when a device is "finished" is partially based on

Exhibit

Verification efforts can significantly outpace projections without solid up-front planning.

System-verification tasks, % of effort spent



how much time is left before it is slated to launch rather than how much time is actually required to ensure reliable functioning of the chip. As a result, bugs are found late, and mask layers need to be regenerated.

By contrast, we have seen verification teams use the data at hand to prioritize various test scenarios associated with particular SOCs. In this way, they can quantify not only the number of tests required to ensure the operability of their intellectual property but also the number required to prove that a component or module does *not* work. One semiconductor player, for instance, used analytics in feasibility discussions about a new integrated-circuit concept. Members of the verification team met with engineers and senior managers to outline their projections of the validation effort and the resources that would be required to bring the device to market. They prioritized the testing scenarios that would need to take place before the device could be deemed done. As issues emerged, the group was able to go back to its plan and, based on the data, recalibrate activities and objectives associated with the development of that integrated circuit. Over time, the team built up a rigorous database of project-verification information; the accuracy of its work-plan projections improved significantly for each successive project.

Simplify the elements to verify

Based on existing project data or user feedback, there may be ways to streamline chip designs or head off performance issues long before verification tasks come into play. In the design-exploration phase, for instance, engineers can consider ways to reuse current intellectual property rather than introduce new intellectual property that might complicate eventual verification efforts. To build the business case for minimizing changes, engineers could review the verification efforts associated with earlier system-on-a-chip tape-outs—the phase in which designers share the photo mask of a circuit for fabrication. Design teams could then categorize SOC projects according to how much (if any) intellectual property was reused and, for each chip or family of chips, compare the verification efforts that were required at the end of development.

When a chip design *does* require new intellectual property, teams can identify and develop the required electronic system–level or C++ verification models early on to ensure that downstream verification is feasible and would not introduce unexpected issues. Before chip design even begins, verification and engineering experts should test the logic embedded in structures that are complex (such as first-in/first-out data structures) or time sensitive (such as arbitration controllers). If testing challenges emerge, the engineers can simplify the designs at the outset, before teams have sunk significant time and resources into the development process. Of course, teams will not have unlimited time and manpower to perform this kind of up-front testing. They may decide to use this approach only when new and critical features are being implemented or only in the development of the most complicated SOCs—such priorities may be determined during early planning discussions, using the data at hand.

Assess the latest verification technology

Verification teams have always had access to a wide range of technologies for creating high-level simulations and prototypes of circuits. There are simulators for testing register transfer–level designs and logic gates. There are hardware-acceleration techniques (also known as emulation techniques) to speed up the verification of large

designs. But newer tools have emerged that allow for robust, mixed-signal simulation so that digital and analog design components can be verified together. And next-generation emulators can operate at higher speeds and handle even larger designs.

The technology has improved; still, none of these approaches, on its own, is a panacea for companies' inability to find design flaws early and release bug-free products. Simulation, the least expensive approach, can be too slow for large designs. Emulation is faster but more costly. Prototyping can provide immediate test results but may be prohibitively expensive for some companies—particularly smaller semiconductor players.

To take advantage of new technologies but keep costs in check, companies can use basic emulation techniques instead of prototyping, and they can exploit cosimulation tools that simultaneously model hardware and software functions to verify hardware and relevant portions of software code. Small semiconductor players may also want to explore the use of cloud-based servers and computing infrastructures, which are provided these days by a number of electronic-design-automation vendors. Third-party IT resources may be particularly useful during tape-out periods, which typically constitute crunch time for smaller project teams: they need the extra computing power for managing tape-out tasks but not during normal work periods, so many consider it a waste to build out large computing infrastructures that would be underused much of the time. To ensure that design data would not be compromised, semiconductor players would need to work closely with third-party platform and service providers to establish rules and protocols for creating secure cloud-based environments.

Larger companies with deeper pockets and pools of talent should attempt to push the technology envelope further—for instance, using mixed-signal simulation as well as virtual-testing platforms in their verification processes. Mixed-signal simulations can generate relatively accurate, cost-effective results, given the faster simulation speeds now possible. Engineering teams may still need to prototype new devices or portions of a system on a chip, but even in those instances, they can use mixed-signal simulation to improve the accuracy of their findings.

In fact, semiconductor companies of any size could realize great cost savings and productivity benefits by making virtual platforms an integral part of their SOC planning and design cycles. The common platform, which would be used for setting goals and for overseeing progress toward those objectives, could help mitigate the need for rework as a chip moves along the production track. Software and hardware engineers could collaborate from the outset on SOC design stages, which would have a favorable impact on verification stages downstream and could allow semiconductor players to close the specification phase of SOC development much faster. Having a virtual platform allowed the engineering team at one semiconductor company to accelerate its software development and have it ready for ramping up and debugging the underlying silicon when the hardware became available. The company had just transitioned from being a hardware provider to a being software-and-services provider, and the virtual platform allowed it to ensure that customer use cases in system- and application-level scenarios were factored into the verification process, which in turn allowed it to reduce the number of iterations required and hence the overall cost and time for development.

Establish the right organization

When it comes to organizing their verification efforts, organizations should have a centralized way to manage verification methodology and architecture development. Activities in these areas should be under the direction of a senior verification leader, aided by a small team, who collaborates with various stakeholders in the organization. He or she should delineate verification standards—giving teams clear targets and well-defined outcomes while affording them the freedom to use the approach that works best to meet those standards. In this way, the leader can encourage teams to think strategically and make decisions based on a common, company-wide understanding of objectives rather than project teams' sometimes insular understanding of what needs to be accomplished.

Additionally, companies may want to create a centralized team for system-verification tasks but maintain a decentralized one for the module-verification tasks that are part of intellectual-property design and development. Consider the development of a wireless system on a chip: the teams responsible for designing the individual radio-frequency and baseband modules would also be responsible for verifying those parts of the chip, but a central systems team should take charge of verifying the transfer of data among these and other modules. The module-level team would require engineers skilled in intellectual-property function and protocols for intellectual-property verification. The system-level team, by contrast, would need engineers familiar with chip architecture, applications, and customer use cases for system verification.

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Future system-on-a-chip advances could be at risk if semiconductor companies fail to address the current verification crunch. Lacking an intervention, SOC projects could end up devouring so many resources that only a few major players can still afford to play the game. But while the SOC verification challenge is real, it may also provide opportunities for semiconductor companies to differentiate themselves competitively in the marketplace. They can use these ideas to reduce both their costs and time to market while ensuring high levels of product quality. In the fast-moving semiconductor industry, that combination could be unassailable.

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